I2C — two-wire shared bus (many chips, few pins)

Inter-Integrated Circuit · synchronous · multi-drop + addressed

HOW IT WORKS

Just TWO wires shared by every chip on the bus: a data line and a clock. Each chip has a unique ADDRESS. The master sends "I want to talk to address 0x60" and only that chip responds. Half-duplex (one direction at a time on the single data wire).

THE WIRES

SDA = data (shared) · SCL = clock (shared)
Both need PULL-UP resistors (open-drain: chips only pull LOW)
+ each chip's address pins set its 7-bit address

KEY FACTS

Speeds: 100 k / 400 k / 1 MHz. Only 2 wires for the whole bus.
Addressing means no chip-select wires — add chips almost free.
Slower than SPI; the pull-ups + addressing add a little overhead.

WHY IT NEEDS PULL-UPS

Chips can only pull the line DOWN (open-drain); the pull-up resistor pulls it back UP. That's what lets many chips share one wire safely without fighting each other.

WHERE WE USE IT

We use I2C where pins are scarce and speed isn't critical: the MCP4728 DAC (CV-out), the MCP23017 (Kill Grid's 16 I/O on 2 wires), and the OLED on the Brain. 2 wires to add a whole 16-channel expander is exactly the trade I2C is for.